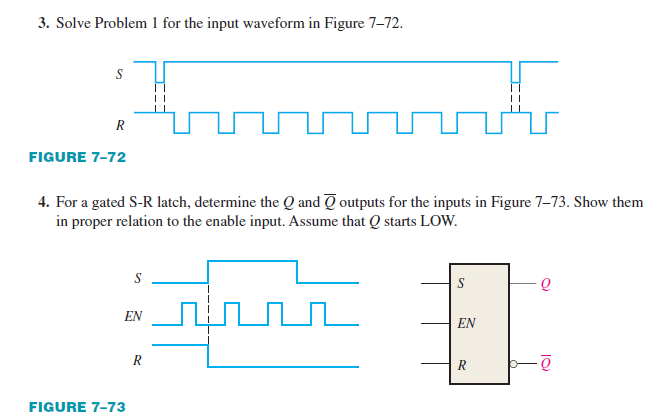
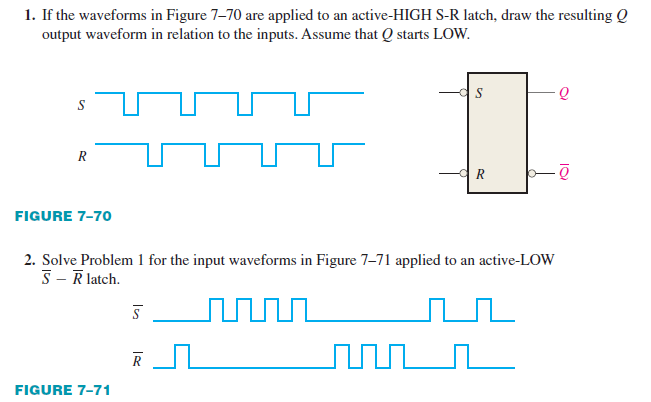
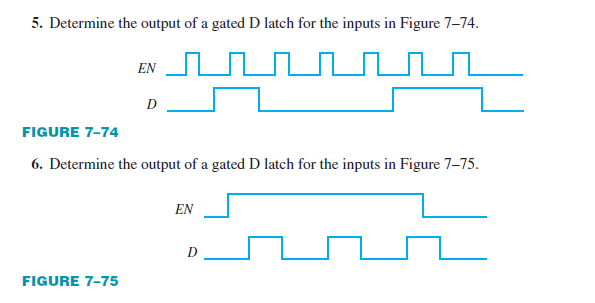
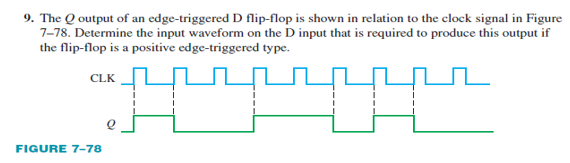
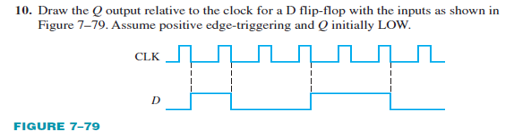
Assignment 5 [Due Date: 28 May]

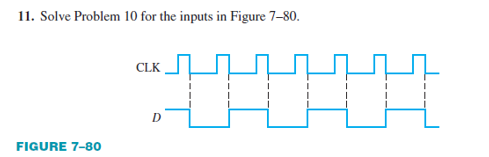
Solve and submit the following questions as your assignment 5. Rest of the questions are for your practice.

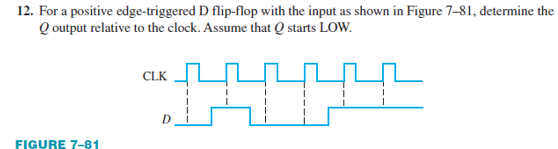
[Assignment questions: 6,9,10,14,17,20,21,23,25]

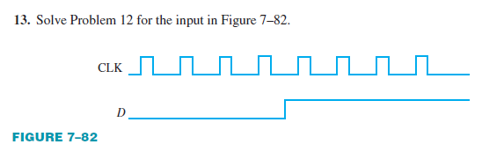


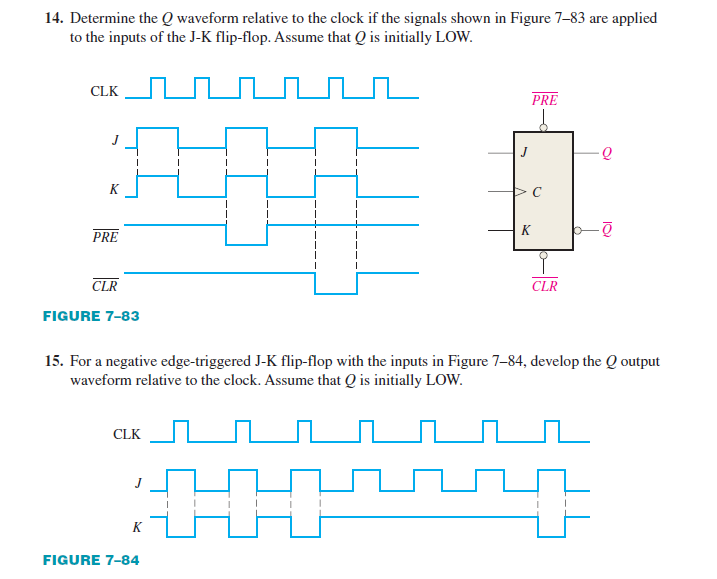


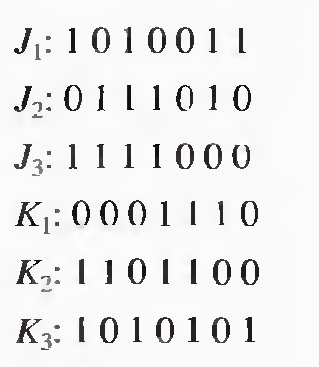
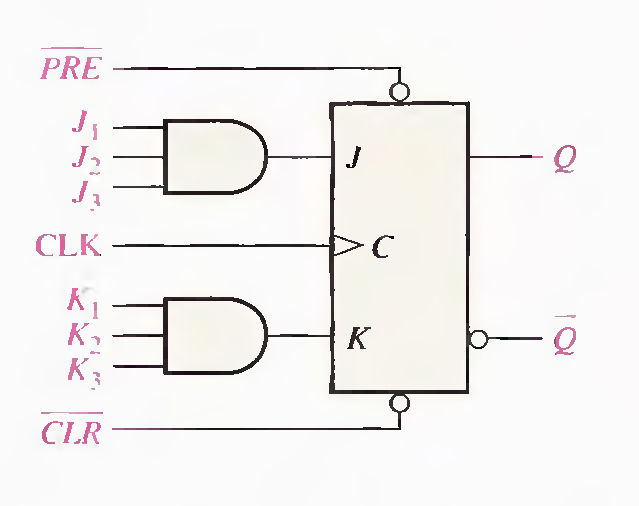




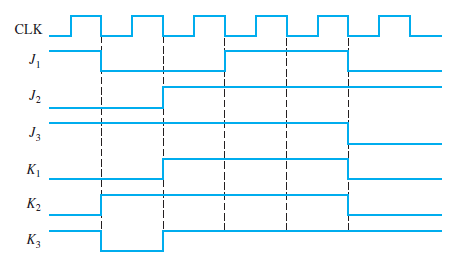




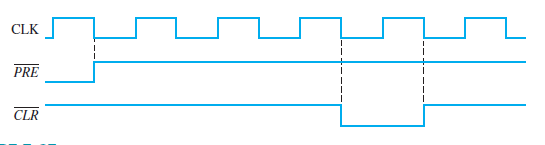
1. The following serial data are applied to the flip-flop through the AND gates as indicated in Figure. Determine the resulting serial data that appear on the Q output. There is one clock pulse for each bit time. Assume that Q is initially 0 and that PRE and CLR are HIGH. Rightmost bits are applied first.

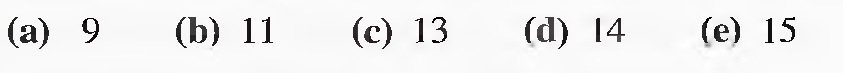
1. For the circuit in Figure -1, complete the timing diagram in Figure 2 by showing the Q output (which is initially LOW). Assume PRE and CLR remain HIGH.



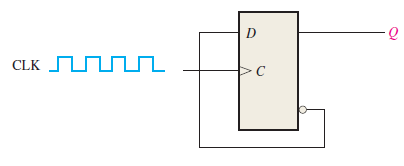
1. Solve Problem 2 with the same J and K inputs but with the PRE and CLR inputs as shown in Figure 3 in relation to the clock.



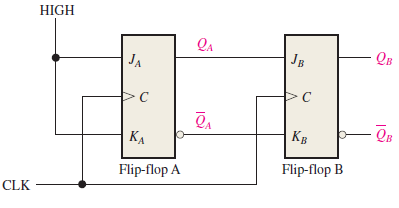
1. Show how to connect a 4-bit asynchronous counter for each of the following moduli. Also for 30kHz clock determine the frequency at the output of each counter.

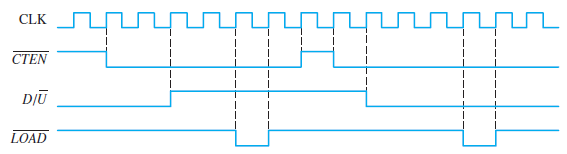


1. A D flip-flop is connected as shown in Figure 7–90. Determine the Q output in relation to the clock. What specific function does this device perform?

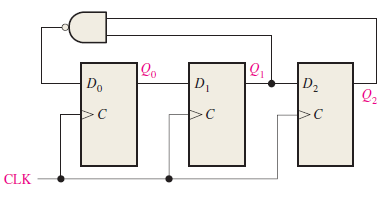


1. For the circuit in Figure, develop a timing diagram for eight clock pulses, showing the QA and QB outputs in relation to the clock.

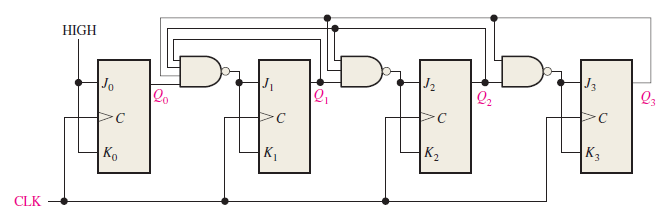


1. Show a complete timing diagram for a 3-bit up/down counter that goes through the following sequence. Indicate when the counter is in the UP mode and when it is in the DOWN mode. Assume positive edge-triggering. 0, 1, 2, 3, 2, 1, 2, 3, 4, 5, 6, 5, 4, 3, 2, 1, 0
2. **Develop t**he Q output waveforms for a 74HC190 up/down counter with the input waveforms shown in Figure. A binary 0 is on the data inputs. Start with a count of 0000.
   1. 

**24. Determine** the sequence of the counter in Figure.

* + 1. 

**25. Determine** the sequence of the counter in Figure 9–74. Begin with the counter cleared.

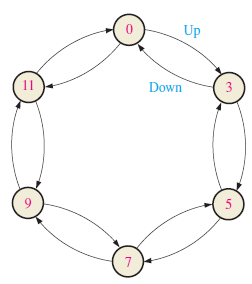
* + 1. 

**26. Design a counter** to produce the following sequence. Use J-K flip-flops. 00, 10, 01, 11, 00, ….

**27. Design a counte**r to produce the following binary sequence. Use J-K flip-flops. 1, 4, 3, 5, 7, 6, 2, 1, ….

**28. Design a counte**r to produce the following binary sequence. Use J-K flip-flops. 0, 9, 1, 8, 2, 7, 3, 6, 4, 5, 0, …

**29. Design a binary** counter with the sequence shown in the state diagram of Figure. (using D flip flop)

* + 1. 

**30. Design** a counter by using D -flip flop only with the irregular binary count sequence shown in the state diagram of Fig. Include Next-state table, transition table, Karnaugh maps and final circuit. 